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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,391	04/19/2004	Hideki Takahashi	252069US2	9709

22850 7590 02/08/2007

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,391	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-17* is/are pending in the application.

4a) Of the above claim(s) *7-12,16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

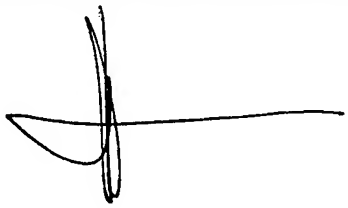
In view of the appeal brief filed on October 16, 2006, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:



Election/Restrictions

Claims 7-12, 16, and 17 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention or species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on July 5, 2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 6, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai (US Pat. 5,270,230) in view of Tanaka (US PGPub 2001/0040255).

Regarding claims 2 and 3, Figure 3 of Sakurai discloses an insulated gate bipolar transistor (IGBT) comprising: a semiconductor substrate of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom surface); an insulated gate transistor 6/7 formed in a region of said substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region 4 of a second conductivity type (p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said substrate; a first main electrode 9 formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface; a first semiconductor layer 2 of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second semiconductor layer 1 of said second conductivity type formed on said second main surface of said substrate and facing said insulated gate transistor; and a

second main electrode 10 formed on said first semiconductor layer and said second semiconductor layer, wherein an interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer is parallel to said first main surface, a distance between said first main surface and said interface is equal to 200 μm, a first interface between said first semiconductor layer and said second main electrode occupies 20-70% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer, and a second interface between said second semiconductor layer and said second main electrode occupies 30-80% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer. Note that Figure 3 of Sakurai shows the interface of the first semiconductor layer 2 occupies approximately 50% of the total area. The difference between Sakurai and the claimed invention is a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 μm or smaller. Figure 10 of Tanaka discloses an IGBT with first and second semiconductor regions (12 and 2B, respectively) in a second main surface of a semiconductor substrate 1, wherein the thickness of the second semiconductor region 2B is less than 1 micron (approximately 0.8 microns) (paragraph [0187]). As shown in Figure 10, region 12 is thinner than region 2B, therefore the first semiconductor region 12 is also less than 1 microns. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Sakurai by using a thickness of less than 1 micron for the first and second semiconductor regions as taught by Tanaka. The ordinary artisan would have been motivated to modify Sakurai in the manner described above for the purpose of

reducing the carrier injection coefficient and increasing the turn-off speed of the device (paragraph [0190] of Tanaka).

Regarding claims 6 and 15, Figure 3 of Sakurai discloses said IGBT functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device shown in Figure 3 of Sakurai has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai in view of Tanaka as applied to claims 2 and 3 above, and as evidenced by Akiyama et al. ("Effects of Shorted...", hereinafter Akiyama).

Regarding claims 4 and 13, a further difference between Sakurai and the claimed invention is a total width of a first width of said first semiconductor layer and a second width of said second semiconductor layer which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is in a range from 50 μm to 200 μm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Sakurai to have a total width within the claimed range, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Figure 1a and 3 and Table 1 of Akima disclose varying the widths of the semiconductor layers in contact with the collector electrode affects device parameters (such

as on-state voltage). Akima demonstrates the total width of the first and second semiconductor layers is recognized in the art as a result effective variable. Since no evidence of unexpected results has been provided, the claimed range is held to be obvious.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai in view of Tanaka as applied to claims 2 and 3 above, and further in view of Reznik (US Pat. 6,798,040).

Regarding claims 5 and 14, a further difference between Sakurai and the claimed invention is an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer. Figure 1 of Reznik discloses an IGBT with an additional semiconductor layer (buffer layer) 6 between the semiconductor substrate 1 and the base region 4, wherein the impurity concentration of layer 6 is greater than that of the substrate 1. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Sakurai by including the additional semiconductor layer (buffer layer) of Reznik for the purpose of elevating the charge carrier density in the region, thereby reducing the switching losses (col. 3, lines 4-8).

Claims 2, 3, 6, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsudai et al. (US PGPub 2002/0048855, hereinafter Matsudai) in view of Tanaka.

Regarding claims 2 and 3, Figure 2 of Matsudai discloses an IGBT comprising: a semiconductor substrate 11 of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom surface); an insulated gate transistor 20/19A formed in a region of said substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region 14/16 of a second conductivity type (p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said substrate; a first main electrode 18 formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface; a second semiconductor layer 10 of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; and a second main electrode 21 formed on said first semiconductor layer and said second semiconductor layer, wherein an interface between said second main electrode and said second semiconductor layer is parallel to said first main surface, a distance between said first main surface and said interface is less than 200 μm, and a thickness of the second semiconductor layer is less than 2 μm. Note that Matsudai discloses region 10 is 1.0 μm thick (paragraph [0050]), region 12 is 15 μm thick (paragraph [0059]), region 13 is 52.5 μm thick (paragraph [0059]), and region 17 is 4.5 μm thick (paragraph [0062]). Therefore, the total thickness is less than 200 μm. The difference between Matsudai and the claimed invention is an

n-type first semiconductor layer formed on the second surface of the substrate, wherein a thickness of each of the first and second semiconductor layers is equal to 2 μm or smaller, a first interface between said first semiconductor layer and said second main electrode occupies 20-70% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer, and a second interface between said second semiconductor layer and said second main electrode occupies 30-80% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer. Figure 10 of Tanaka discloses an IGBT with first semiconductor regions 12 (n-type) and second semiconductor regions 2B (p-type) in a second main surface of a semiconductor substrate 1, wherein the thickness of the second semiconductor region 2B is less than 1 micron (approximately 0.8 microns) (paragraph [0187]). As shown in Figure 10, region 12 is thinner than region 2B, therefore the first semiconductor region 12 is also less than 1 microns. Figure 10 of Tanaka also discloses a first interface between said first semiconductor layer 12 and electrode 3 occupies approximately 20-70% of interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer; and a second interface between said second semiconductor layer 2B and said electrode 3 occupies approximately 30-80% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Matsudai by using first and second semiconductor regions with thickness of less than 1 micron and the specified width as taught by Tanaka. The ordinary artisan would have been motivated to modify Matsudai in the manner described above for the purpose of reducing

the carrier injection coefficient and increasing the turn-off speed of the device (paragraph [0190] of Tanaka).

Regarding claims 6 and 15, after the above combination, the IGBT of Matsudai and Tanaka functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device of the above combination has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsudai in view of Tanaka as applied to claims 2 and 3 above, and as evidenced by Akiyama et al. ("Effects of Shorted…", hereinafter Akiyama).

Regarding claims 4 and 13, a further difference between Matsudai and the claimed invention is a total width of a first width of said first semiconductor layer and a second width of said second semiconductor layer which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is in a range from 50 μm to 200 μm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Matsudai to have a total width within the claimed range, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Figure 1a and 3 and Table 1 of Akima disclose varying the widths of the semiconductor layers in contact with the collector electrode affects device parameters (such

as on-state voltage). Akima demonstrates the total width of the first and second semiconductor layers is recognized in the art as a result effective variable. Since no evidence of unexpected results has been provided, the claimed range is held to be obvious.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsudai in view of Tanaka as applied to claims 2 and 3 above, and further in view of Reznik (US Pat. 6,798,040).

Regarding claims 5 and 14, a further difference between Matsudai and the claimed invention is an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer. Figure 1 of Reznik discloses an IGBT with an additional semiconductor layer (buffer layer) 6 between the semiconductor substrate 1 and the base region 4, wherein the impurity concentration of layer 6 is greater than that of the substrate 1. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Matsudai by including the additional semiconductor layer (buffer layer) of Reznik for the purpose of elevating the charge carrier density in the region, thereby reducing the switching losses (col. 3, lines 4-8).

Claims 1, 2, 3, 6, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Sakurai.

Regarding claims 2 and 3, Figure 10 of Tanaka discloses an insulated gate bipolar transistor (IGBT) comprising: a semiconductor substrate 1 of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom); an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region 7 of a second conductivity type (p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate; a first main electrode 11 formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface; a first semiconductor layer 12 of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second semiconductor layer 2B of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second main electrode 3 formed on said first semiconductor layer and said second semiconductor layer; wherein an interface between said second main electrode and each of said first and second semiconductor layers is parallel to said first main surface, a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 microns or smaller (0.8 microns) (paragraph [0187]); a first interface between said first semiconductor layer 12 and said second main electrode 3 occupies approximately 20-70% of

said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer; and a second interface between said second semiconductor layer 2B and said second main electrode 3 occupies approximately 30-80% of said interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer. Tanaka does not specifically disclose a distance between said first main surface and said interface is equal to 200 microns or smaller. Figure 3 of Sakurai discloses an IGBT with a substrate thickness of 200 μm. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Tanaka by using the substrate thickness of 200 μm as taught by Sakurai for the purpose of selecting a thin substrate, allowing for a thin drift region. Alternatively, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a distance between the first surface and the interface equal to or less than 200 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). The disclosure of Sakurai is evidence that the thickness of the substrate is a result effective variable (see col. 2, lines 47-51).

Regarding claims 6 and 15, Figure 10 of Tanaka discloses said IGBT functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device shown in Figure 10 of Tanaka has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Sakurai as applied to claims 2 and 3 above, and as evidenced by Akiyama et al. ("Effects of Shorted...", hereinafter Akiyama).

Regarding claims 4 and 13, a further difference between Tanaka and the claimed invention is a total width of a first width of said first semiconductor layer and a second width of said second semiconductor layer which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is in a range from 50 μm to 200 μm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Tanaka to have a total width within the claimed range, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Figure 1a and 3 and Table 1 of Akima disclose varying the widths of the semiconductor layers in contact with the collector electrode affects device parameters (such as on-state voltage). Akima demonstrates the total width of the first and second semiconductor layers is recognized in the art as a result effective variable. Since no evidence of unexpected results has been provided, the claimed range is held to be obvious.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsudai in view of Tanaka as applied to claim 2 and 3 above, and further in view of Reznik (US Pat. 6,798,040).

Regarding claims 5 and 14, a further difference between Tanaka and the claimed invention is an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer. Figure 1 of Reznik discloses an IGBT with an additional semiconductor layer (buffer layer) 6 between the semiconductor substrate 1 and the base region 4, wherein the impurity concentration of layer 6 is greater than that of the substrate 1. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Tanaka by including the additional semiconductor layer (buffer layer) of Reznik for the purpose of elevating the charge carrier density in the region, thereby reducing the switching losses (col. 3, lines 4-8).

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be

reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

January 29, 2007